Trigger Configuration for the BigBite and HRS-L Spectrometers

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1 Introduction

In the E05-102 experiment we were measuring double-polarized asymmetries in the reactions $^3\vec{He}(\vec{e},e'd)$, $^3\vec{He}(\vec{e},e'p)$ and $^3\vec{He}(\vec{e},e'n)$. For the measurement of the neutron channel $(e,e'n)$ we were using the neutron detector (HAND) in coincidence with the Right High Resolution Spectrometer (HRS-R). For the $(e,e'p)$ and $(e,e'd)$ channels we were using the BigBite Spectrometer in coincidence with the Left High Resolution Spectrometer. My mission was to assemble the electronics for the coincidence trigger between BigBite and HRS-L. In this report I will briefly describe the trigger construction. Before and during the experiment I made a series of checks with an oscilloscope and simulated pulses. As a result of those tests I got a lot of signal traces which can be now compared with the trigger schematics in order to see if the triggers work properly. Another set of tests was made during the production running using the TDC and scaler data from all the triggers. Using this information we were able to check if the real triggers work the way tried to design them.

2 BigBite Spectrometer

BigBite spectrometer is a large momentum- and angle-acceptance spectrometer. It was originally used in NIKHEF and was brought to Jefferson Lab in 2003. It consists of a single normal-conducting dipole magnet (see figure 1 below) and a detector package. The maximum magnetic field in the spectrometer is 0.92T (at current 510A), which enables the detection of the particles with momentum $< 700 MeV/c$. The hadron detector package consists of two Multiwire Drift Chambers and two scintillator planes. Both scintillator planes are made of 24 scintillator paddles each approximately 8cm wide (see figure 1). The first (dE)-scintillation plane is 3mm thick while the second (E)-plane is made of 3cm thick material. The photons from each paddle are read with two Photonis XP 2262B Photomultipliers attached to each side of the paddle. The basic characteristics of the spectrometer can be found in table 1.

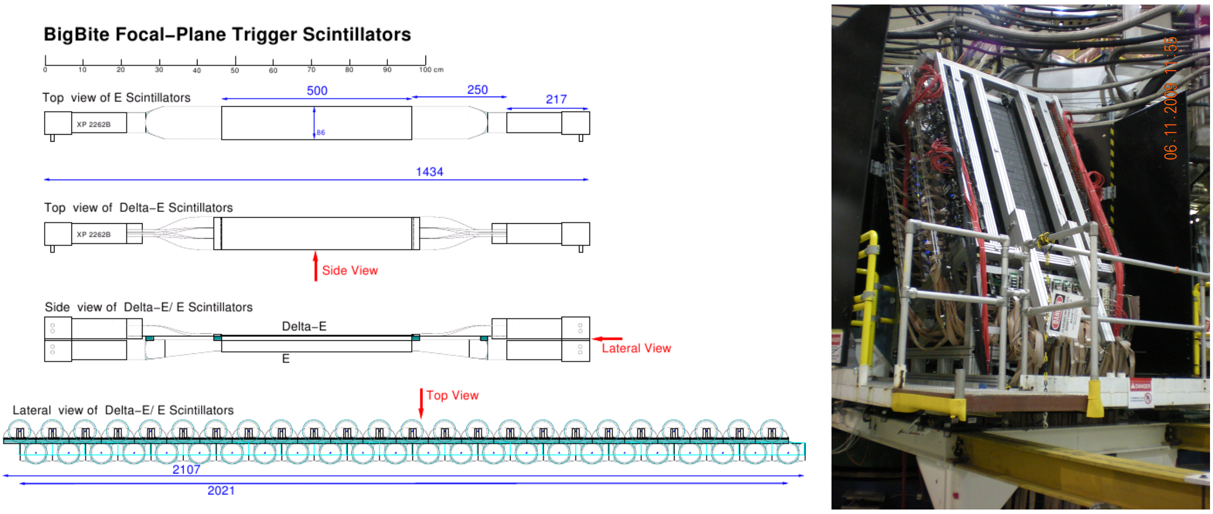

Figure 1: *Left:* Schematics of the Scintillator counters used for the BigBite trigger detector; *Right:* Picture of the BigBite Spectrometer. Scintillator planes are clearly seen on the back of the spectrometer.

BigBite characteristics	
Configuration	Dipole
Momentum range	$200 - 900$ MeV
Momentum acceptance	$-0.6 \leq \frac{\delta p}{p} \leq 0.8$
Momentum resolution	4×10^{-3}
Angular acceptance	≈ 100 msr
Angular resolution	≈ 1 msr

Table 1: Main characteristics of the Big Bite spectrometer. It has a large momentum and angular acceptance which makes it a great device for the detection of the quasi-elastic hardons [1].

3 HRS-L and Bigbite Triggers

Triggers are electronic pulses that tell us when a particle hits the detector or a detector package in a spectrometer. From the combination of these signals at a given moment we decide whether they correspond to a certain physical process and whether they should be recorded or not. This means that only after the trigger is accepted we start downloading data from ADC and TDC modules to the disks. All data that were read (saved) after one accepted trigger are called an event. In our experiment (E05-102) we had seven different triggers for the combination of the BigBite and HRS-L spectrometers.

3.1 Trigger T1:

Trigger T1 is the BigBite main trigger. It is triggered whenever we get a valid hit in one of the paddles of the E-scintillation plane. Its complete electronics scheme is shown in figure 2. The signals from the PMTs are led from the detector patch panel (PP) to the patch panel in the BigBite weldment where all the electronics is situated. For that we used 30 m coaxial cables. Once in the weldment all 48 signals were lead to the analog amplifiers where they were multiplied by a factor of 10. For the multiplication we used Phillips modules PS-776. Then we led amplified signals over 8ns LEMO cables to discriminators. We used LeCroy LC-3412 modules with electronically controlled threshold which enabled us to remotely control the threshold during the experiment. We used twisted-pair ribbon cables to connect the discriminators with the LeCroy logical units LC-4516 where we first made a logical AND[1] between the signals from the left and right PMTs from each scintillation paddle

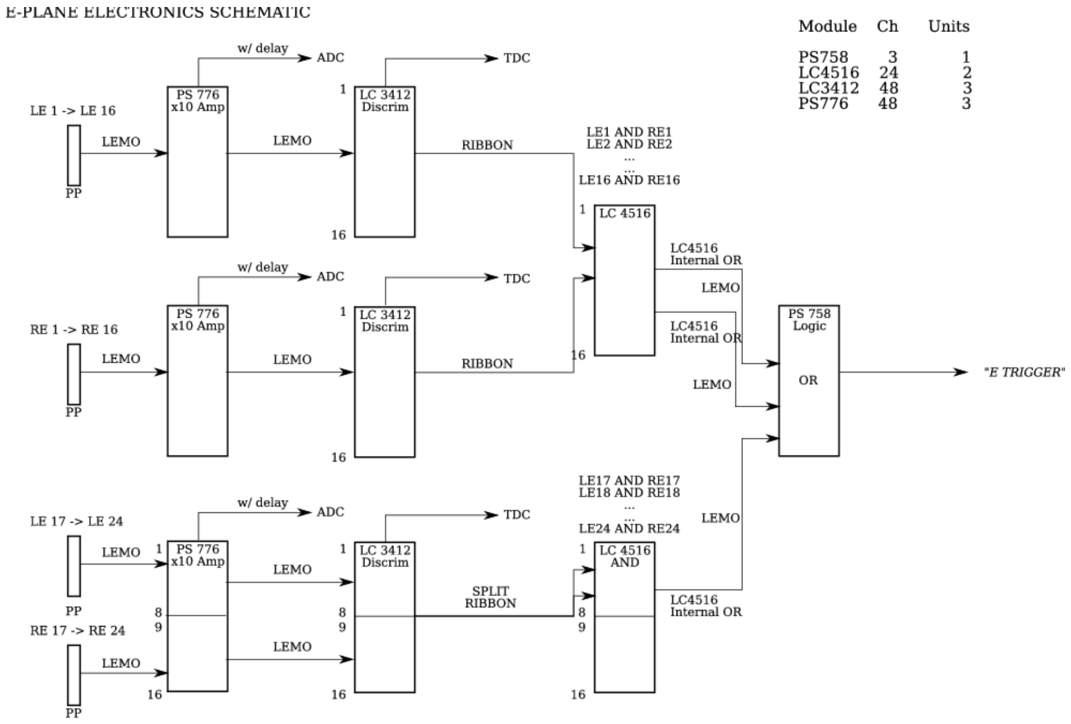

Figure 2: First part of the electronics scheme of trigger T1.

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[1] In our experiment we decided that a valid hit in the E-plane should have pulses in both left and right PMTs.

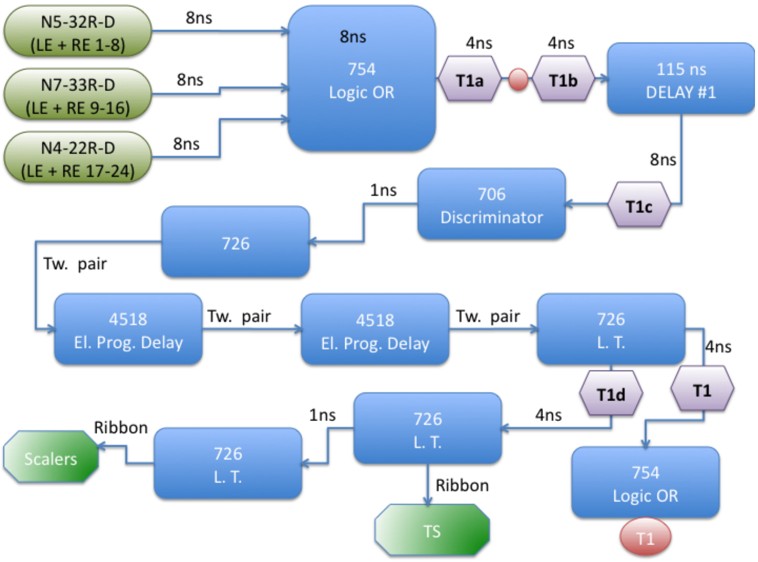


Figure 3: First part of the electronics scheme of trigger T1.

and then a logical OR between all the channels. Since our detector has 24 PMTs (channels) we have to use two LC-4516 modules with sixteen channels. On the output of these two modules we got three signals, each representing an OR between eight paddles. We then led these three signals over 8ns LEMO cables to the Philips module PS-754 where we made a final logical OR between these signals and in the end got the T1-trigger pulse.

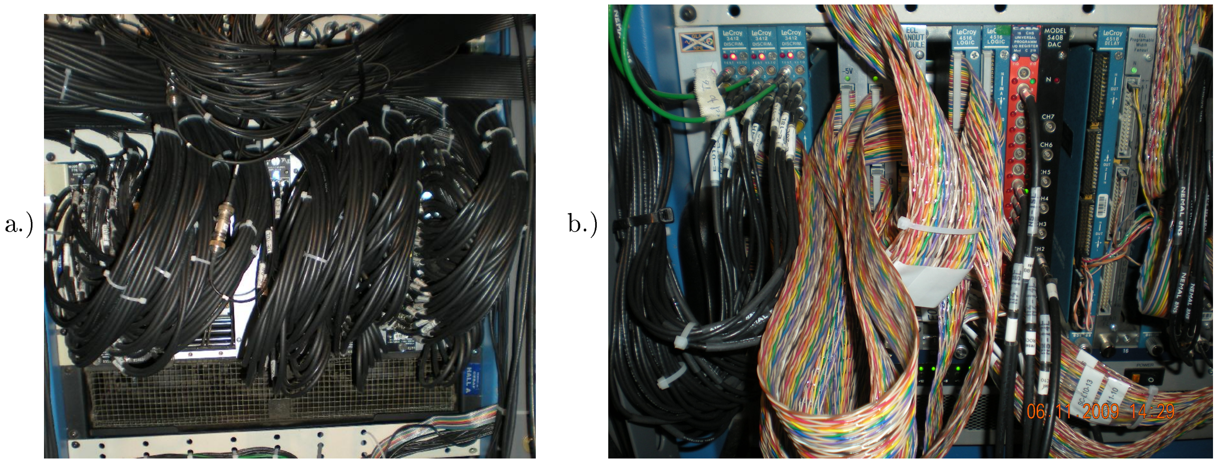


Figure 4: Trigger T1 electronics. *a.)* Analog amplifiers, where signals from PMTs are amplified by factor 10. *b.)* Three discrimination modules LC-3412

We also had to consider the possibility that Trigger pulses from the detectors do not all arrive at the same time. It turned out that in order to be able to form a coincidence trigger with the left arm, an additional delay had to be applied to trigger T1. For that we used two electronically programmable delay modules, each being able to delay signal for 32 ns. This has given us the ability to control and adjust the delays remotely during the experiment. Level-translation modules PS-726 were places before and after the programmable delay modules in order to translate the LEMO-cable signals to twisted-pair signals. For the rest of the needed delay we used ordinary 115ns cable delay. To refresh the signal, after it comes out of the long cable, we used the PS-706 discriminator.

3.2 Trigger T2:

Trigger T2 is a secondary BigBite trigger and is triggered when we have a valid hit in a dE-scintillation plane. When looking at the T2 electronics scheme in figure 5, we can notice that it is constructed a bit differently than the one for trigger T1. After the amplification we do not discriminate the signals and then make logical operations with digital pulses, as we did for the T1-trigger. Instead, we first do the analog sum of the signals from the left and right PMT and then discriminate the sums. This way we also accept those signals from the detector where only one PMT per paddle was hit, as long the detected signal was big enough to come through the discriminator.The main reason for such a construction was to detect particles with very small momenta. To do the sum we used LeCroy LC-428F modules. These modules have two outputs - a capacited and non-capacited. During the debugging process of our electronics we realized that we should use only capacited outputs, otherwise we got 60Hz noise in our signals, caused by the power supply cables. From the output of the discriminators we led the signals to the PS-726 modules, in order to translate the signals from Ribbon to LEMO cables. We then took these wires and attached them to the CAEN module N408 to make a logical OR between them in order to get our T2 trigger.

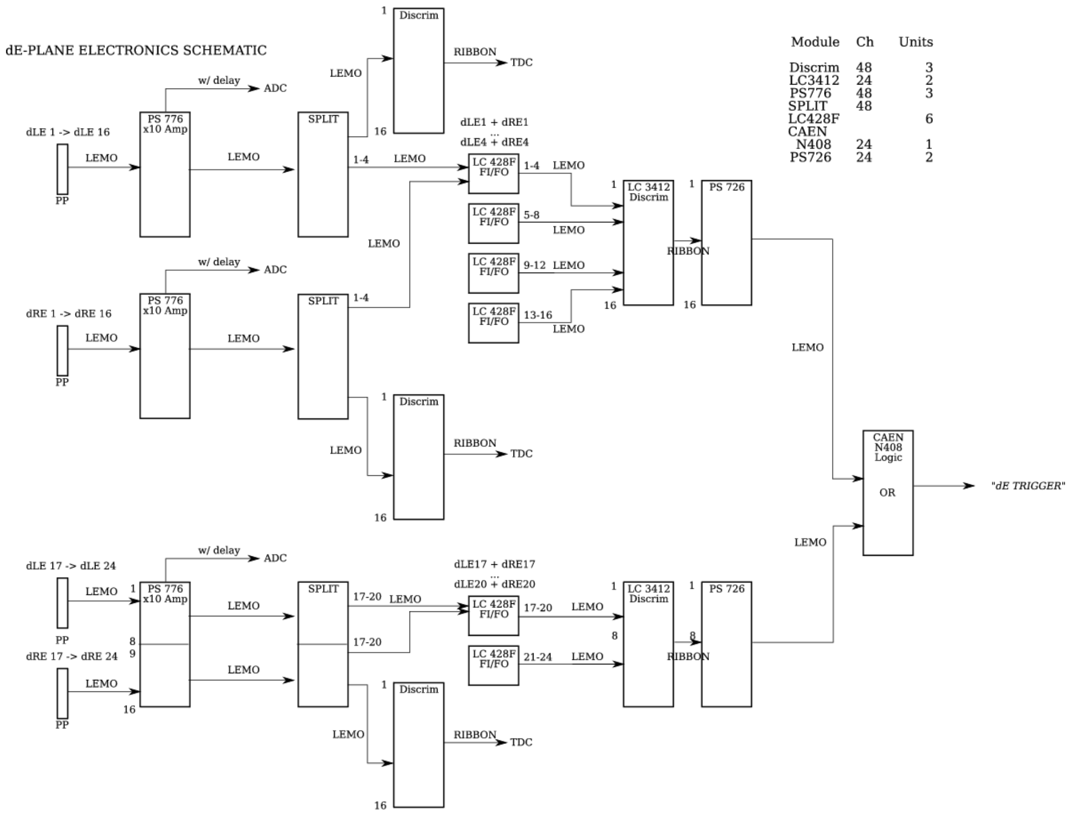


Figure 5: First part of the electronics scheme of the T2 trigger.

Once we had the T2 trigger we also had to apply some additional delay to it. From figure 6 we can see that basically we did the same thing as we did for the T1, but with a bit shorter cable delay, because trigger T2 comes few *ns* after T1. This time difference is caused by additional electronics and cables that we used for the construction of this trigger.

3.3 Triggers T3, T4, T5 and T6:

Triggers T3 and T4 are HRS-L triggers. I will not discuss their construction in detail here. It is enough to know that the T3 trigger is the main trigger and is triggered every time when there are valid signals in both S1- and S2- scintillation planes. Valid signal means that in the hit scintillation paddle both left and right PMTs saw light. Trigger T4 is a supplementary HRS-L trigger and is triggered when only the S1-plane and the Cerenkov

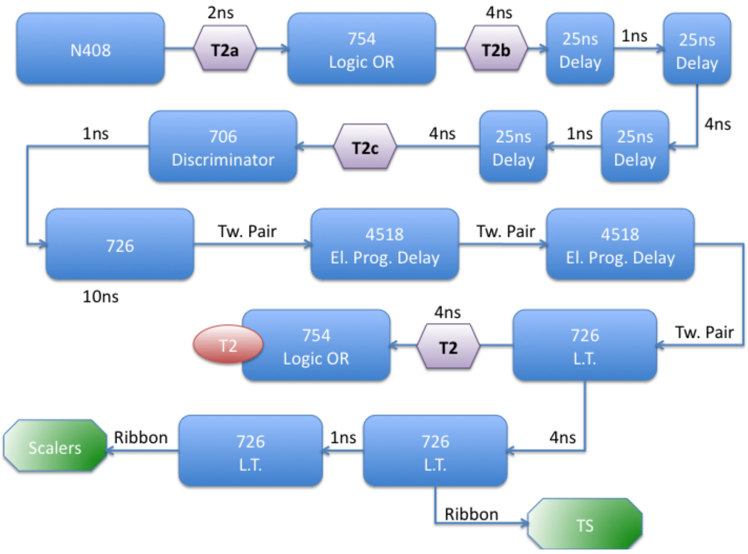


Figure 6: Second part of the electronics scheme of the T2 trigger.

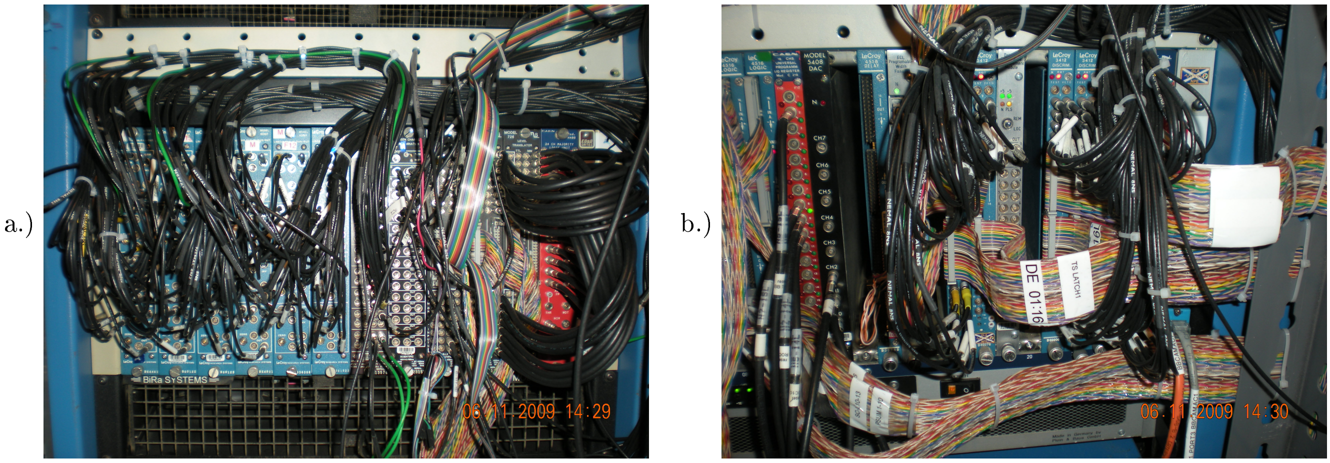


Figure 7: Trigger T2 electronics. *a.)* FI/FO modules LC-428F where we do the sum of the analog signals from left and right PMTs. *b.)* Discrimination modules: Three modules are used for the discrimination of the TDC signals and two for the discrimination of the summed signals.

detector, which is positioned in between the two planes, have valid pulses. This means that we can not have both triggers at the same time - when there is T3 there is no T4 and vice-versa. Because we believed that the majority of our scattered electrons comes through both scintillation planes we did not pay much attention to T4, but only dealt with T3.

Triggers T5 and T6 were our coincidence triggers. We started the construction of these two triggers ambitiously. We considered programmable coincidence window widths as well as the position of the window relative to T1 or T2. However, when we made a simulation of the experiment, we realized that because of the long cables, T3 came too late from the HRS-L and would consequently cause the ADC-gate to come too late to read the pulses from BigBite. Because of that we had to make a much simpler version of the coincidence trigger without any extra features.

Figure 8 shows the scheme of our final coincidence trigger. The coincidence trigger between T1 and T3 was T5 while the coincidence trigger between T2 and T3 was T6 . Trigger T3 from the HRS-L goes first into the

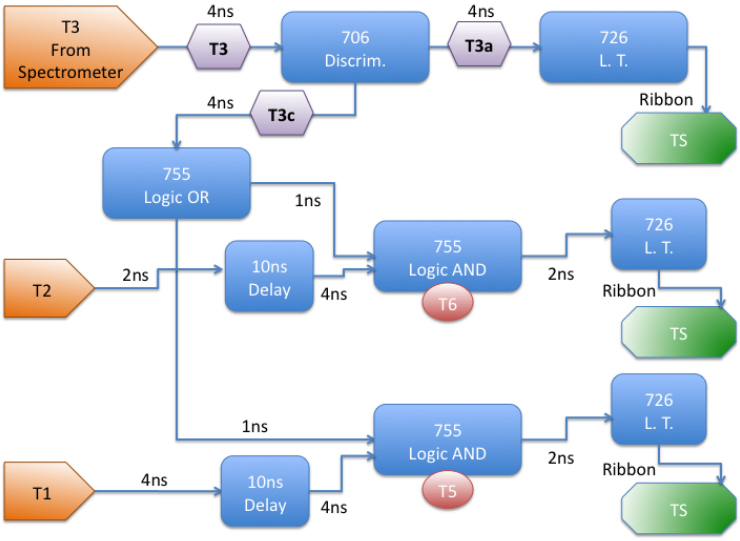


Figure 8: Trigger T5 and T6 schemes.

discriminator in order to refresh the pulses. The output signal is then led to the PS-755 module where we make a coincidence window out of it. We have set the coincidence window to be approximately 80ns wide. Once we had the coincidence window we were able to form coincidence triggers. We simply took two PS-755 modules and made an AND between the coincidence window and the properly delayed T1 and T2 signals. The outputs from these two modules represent coincidence triggers.

3.4 Trigger T7:

During the set-up period, when there was no electron beam available, we were using cosmics to test if the BigBite detectors (especially the MWDCs) work properly. For that purpose we designed a special cosmics trigger, called T7. We put an additional 2m long scintillation bar (HAPPEX paddle) inbetween the two wire chambers. This bar was long enough to vertically cover the MWDC and the Scintillation planes. We used this paddle to check if the particle that hit the dE- and E-planes also managed to come though the MWDC. The signals from the left and right PMT on this paddle were led the same way as all other signals to the BigBite weldment. There we first amplified them and then made a logical OR between them. In the end we formed an AND between this signal and the T1 to get the coincidence cosmics trigger T7. When the real experiment started this additional (HAPPEX) paddle was removed. Therefore there should be no T7 events in the production data.

3.5 Trigger supervisor and Level One Accept pulse:

Once we have all the triggers we need to send them to the Trigger Supervisor (see figure 9). The delays of triggers T1,T2 and T3 are set in a way that they come into the TS at approximately the same time. Triggers T5 and T6 come approximately 30ns later. When signals come to the Trigger supervisor, it decides whenever to accept or reject the given trigger. If it accepts the trigger it returns a Level one accept (L1A) pulse which we then use to start the TDC and ADC read-out.

During the real experiment, the rates of all triggers are not the same due to various reasons: spectrometers have different acceptances, and since we are interested mostly in coincidence events we do not want too many single-arm events. Therefore we can specify the rates with which we want to accept each trigger by setting proper prescale factors. This also enables us to correctly set the total rate of information that we can store so that we do not have too large dead time. At the moment we are limited to 2.5k events per second or approximately 5.5MB per second.

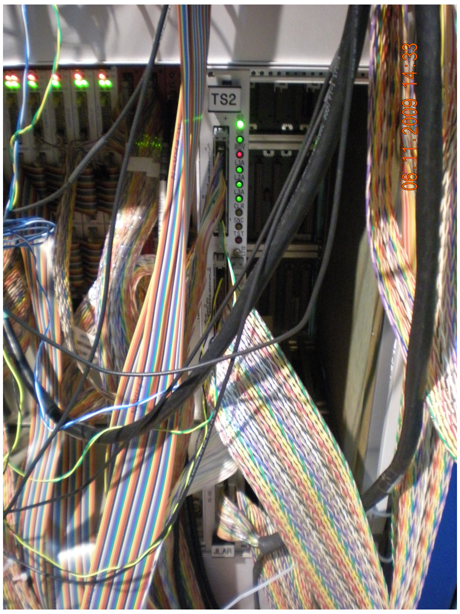


Figure 9: BigBite and HRS-L Trigger supervisor (TS2) with all corresponding cables.

3.6 BigBite Re-Timing

We could use L1A signal directly to start the read-out of the ADCs and TDCs. However, in our experiment we wanted these signals always to be relative to T1 or T2 if they exist. For that we used the additional electronics shown in figure 10. We named this part of electronics BigBite Re-timing. First we use a PS-755 module to form a logical OR between T1 and T2. Delays of these two triggers are set in a way that T1 comes approximately 2ns before T2. This way TDC signals will always be timed off T1, if T1 exists. If there is no T1 then they will be timed off T2. After we made (T1 OR T2) we take this signal through some additional delay. We need this delay because TS2 needs some time to think and decide before sending the L1A signal. The delay is set in a way that L1A always comes before (T1 OR T2). This is the main idea of this circuit. Then we take both signals and put them into another PS-755 module where we make an AND between them to get our final output signal, with which we start the read-out of the ADCs and TDCs.

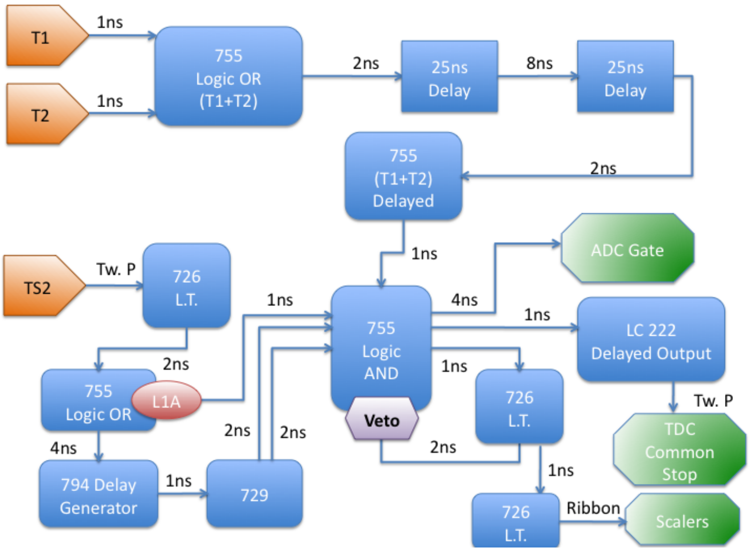


Figure 10: BB-retiming scheme

However, it can also happen that in a given event there is no T1 nor T2 but only T3. Since we would also like to take those events but only when T1 or T2 are truly absent, we added modules PS-794 and PS-729 which delay the L1A signal for approximately 90ns. If there is really no T1 or T2, the circuit decides to take un-timed and delayed L1A. Module PS-755 which makes the final AND is set to setting 2, which means that it makes an AND between any two input signals. In the case of proper events these two singal are L1A and (T1 OR T2). When there is no T1 or T2, then these two signals are two delayed copies of the L1A. However, we need to be careful here. In a case of any proper event we also get a delayed L1A signal that always comes 90ns after the non-delayed one. This would mean that we need to stop reading the input until this signal has ended. Therefore we make a loop and lead a delayed output signal back into the module as a VETO, which prevents the delayed L1A signal from forming a bogus event.

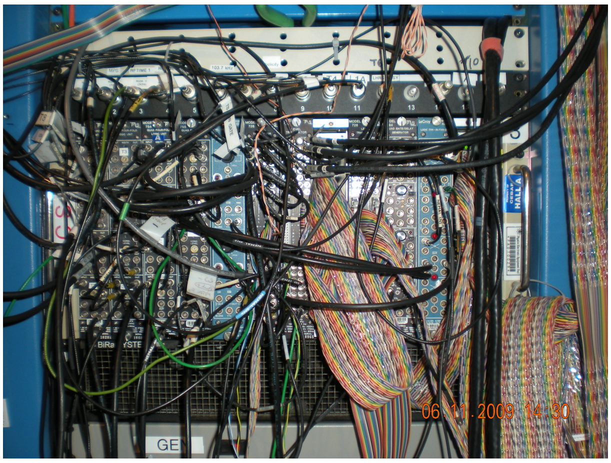


Figure 11: BigBite re-timing electronics.

3.7 BigBite ADCs, TDSs and Scalers

Figure 12: Left figure shows BigBite high resolution TDC modules. Right figure shows CEAN ADC modules

In order to get a deposited energy information from the BigBite PMTs we take a second copy of the amplified signals in modules PS-776 and lead them to the ADC modules where we digitize the analog signals. For the transport of the ADC signals we first used ordinary twisted-pair ribbon cables. However, during the tests we realized that this is not a good choice. The signals in a given wire were strong enough to induce cross-talk signals in neighboring wires. Since this would cause a lot of problems we changed these cables with the ribbon cables made of small coaxial cables. With those cables the induced noise disappeared. We also used hi-pass filters on

the inputs to the ADC modules to get rid of the low frequency (i.e. 60Hz) noise. Looking at figures 2 and 5 we can see that ADC signals before going into the ribbon cables go through some delay. It is very important to delay these signals enough, so that they do not come to the ADC modules before the ADC-window is opened by the BigBite re-timing pulse.The total amount of delay from the output of the amplifier to the input of the ADC module is approximately 500ns. In this experiment we have used CAEN V792 ADC modules shown in figure 12.
Figure 13 shows the scope plots of the ADC window and analog pulses from the dE- and E-planes right before

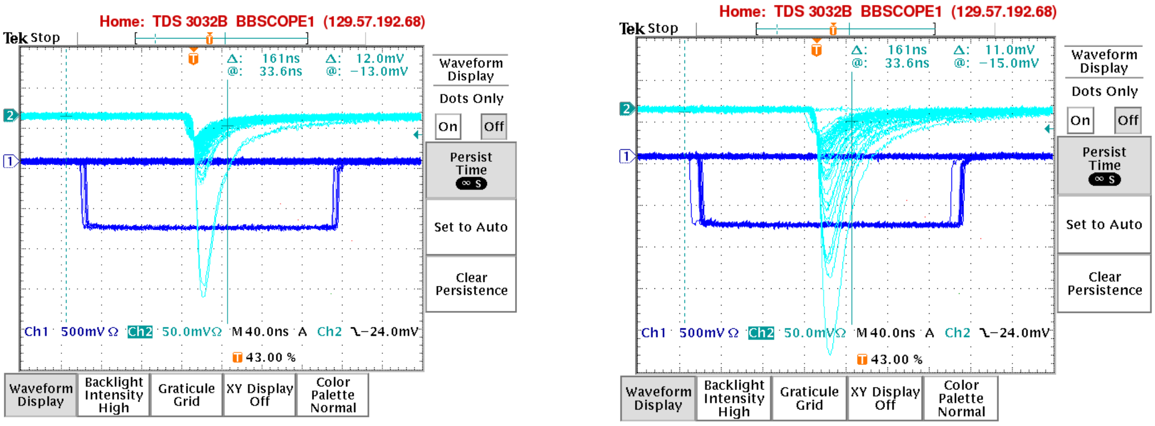


Figure 13: *Left:* Position of the analog signal from the dE-1L PMT relative to the ADC gate. *Right:* Position of the analog signal from the E-1L PMT relative to the ADC gate.

going into the ADC modules. The ADC gate is approximately 250ns wide. For the ADC gate we simply used the BigBite re-timing pulse from the output of the PS-755 module (see figure 10), where we increased the length of the pulse on that module to the correct value.

We are also interested in the time information i.e. when some particles hit a detector relative to the other. For that we have used the F1-TDC modules with resolution of 60ps shown in figure 12. We were running these modules in the common-stop mode. These modules have an acceptance window through which data are constantly flowing. When the common stop signals appears the module reads the data that are currently within its window and stores them. For the common-stop pulse we again used the BigBite re-timing pulse, which was properly delayed using the LC-222 module.

In the case of the E-plane we take signals for the TDCs from the discriminator modules LC 3412 and transport them with ribbon cables to the F1-TDC modules. The dE-plane signals are connected to TDCs somewhat differently. First we use splitters made of resistors to divide the analog signal comming from the amplifiers into two copies. The first copy goes to the FI/FO modules as already mentioned. The second copy goes directly to discriminators and then through the ribbon cables to the TDC modules. Because of the resistor-splitters the signals going to the TDCs have half the initial amplitude. It is very important to consider this when setting the thresholds for discriminators. They should be set to the approximately half of the value used for the E-plane discriminators.

Besides the signals from all the PMT we also decided to connect all triggers to the TDCs. This turned out to be very useful. We were able to monitor the triggers during the experiment to check if they work properly. On the other hand, assuming that triggers work properly, we were directly able to see coincidence peaks and with limited resolution separate deuterons from protons. In this case we used FastBus TDCs with 500ps resolution. In order to monitor the rates at different stages of electronics we attached the relevant signals to the scaler modules. We led to scalers the copies of all 96 TDC signals and the copies of all 48 signals that we get after we perform the logical AND between left and right PMT. We have used these scalers to monitor the operation of all the channels in the scintillation planes. If the rates in one of the channels would be dramatically different than in the others, that would suggest that something is wrong with that channel.

On the other hand, the most important signals led to scalers are the copies of the triggers. Monitoring the trigger rates enables us to correctly set the prescale factors so that the dead time in our data acquisition system is not too big. Through these scalers we can also see if something is wrong with our experiment i.e. the target

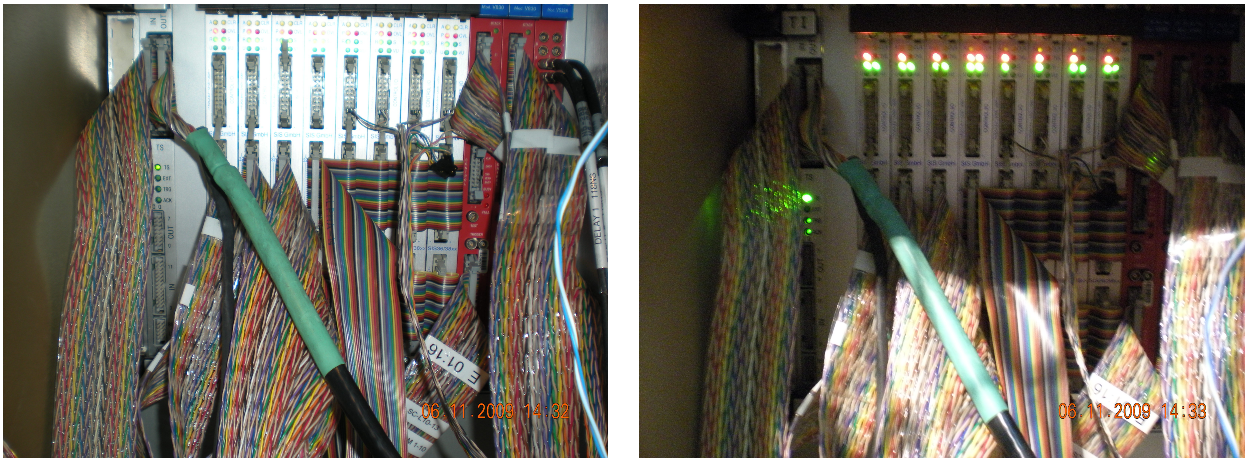
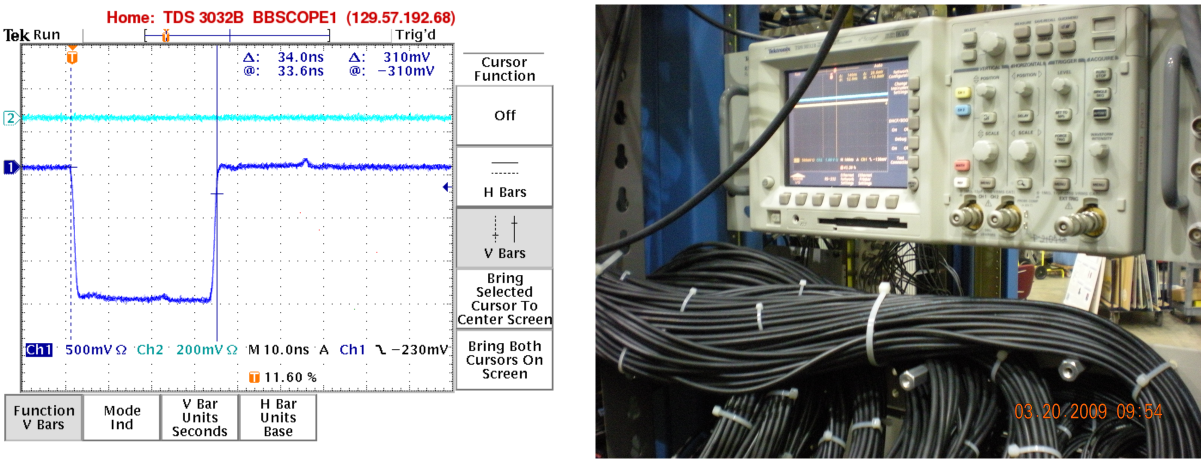


Figure 14: Scaler modules

cell exploded or something happened with the beam. In our experiment we were using a polarized beam as well as a polarized target. Therefore we used four scaler modules to monitor the trigger rates, each for one beam-target setting: $[Beam\ Target] = [++], [-+], [+-], [--]$. Using this technique we were able to estimate the raw asymmetries of our experiment on-line directly from the scalers, without detailed analysis of our data.

4 EDTM tests

In order to test the electronics that we built and to correctly set the delays for each trigger we used artificial signals that simulated real physical processes. For that purpose we used two EDTM modules (Event Dead Time Monitor), one configured as master situated in the HRS-L and the other in the BigBite weldment as a slave. The master EDTM sends out simulated pulses to the HRS-L, electronics and one pulse to the slave-EDTM. The slave module is programmed in a way that sends the simulated signals to the BigBite electronics with the delay which corresponds to the real physical delay. For that we had to consider the difference in flight paths and flight times of the proton and the electron, as well as the length of the cables going from HRS-L to the BigBite weldment.


Home: TDS 3032B BBSCOPE1 (129.57.192.68)

Tek Run Trig'd

Δ: 34.0ns Δ: 310mV
@: 33.6ns @: −310mV

Ch1 500mV Ω Ch2 200mV Ω M 10.0ns A Ch1 ⌄ −230mV

11.60 %

Figure 15: *Left:* The width of the EDTM pulse, going into the discriminators and FI/FO modules. *Right:* Textronix oscilloscope TDS2012B.

For the E-plane we connected the EDTM signals to the test inputs of the LC-3412 discriminators. In the case of the dE-plane we plugged the EDTM signal as an extra input to the FI/FO modules LC-428F. We set the EDTM modules to send out signals at approximately 20 Hz. Once we had the simulation running we were able to check our electronics. For that we used the two-channel Tektronix Oscilloscope TDS2012B shown in figure 15, which supports an Ethernet connection. Therefore we were able to store the scope screen shots over the Internet and later compare them with the electronics schematics described in this paper. Figures 16 to 40 show various scope plots that we made during our tests and short descriptions of how well they agree with the schematics.

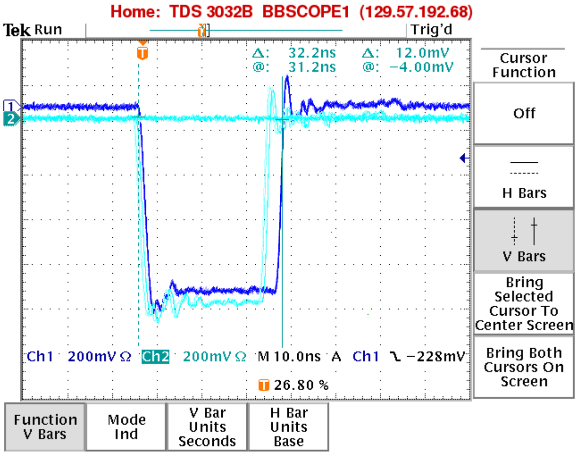


Figure 16: Plot shows the time difference between T1s(cyan) and T3s(blue) on the input to the scalers. We can see, that both triggers come to the scalers at approximately the same time (difference is smaller than 1ns)

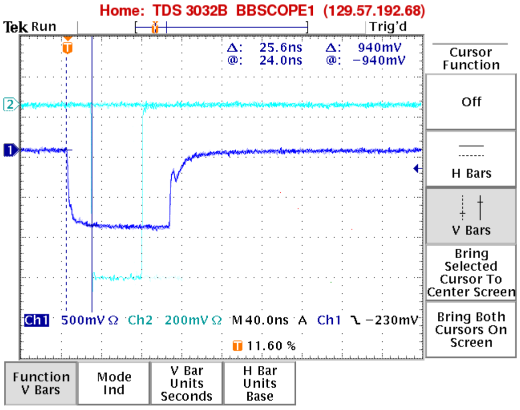


Figure 17: This plot shows time difference between trigger T1(cyan) on the output from module PS-755 and trigger T3(blue) on the end of the cable from HRS-L. Time difference between the two is 26ns. Looking at figures 3 and 8 we see that T3-to scalers comes $4+10+4+5 = 23ns$ after T3 and that T1-to scalers comes $5-3ns$ before T1. That means that according to schematics T1 also comes $23+3 = 26ns$ after T3.

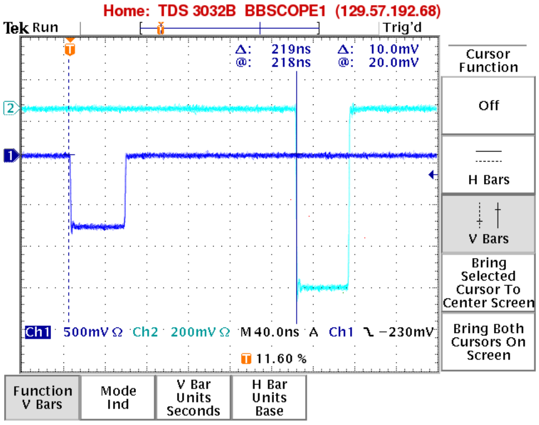


Figure 18: Plot shows the time difference between the output from the PS-754 module (figure 3) where we make an OR between the signals from the LC-4516 module and trigger T1 output. Time difference was set to be 219 ns

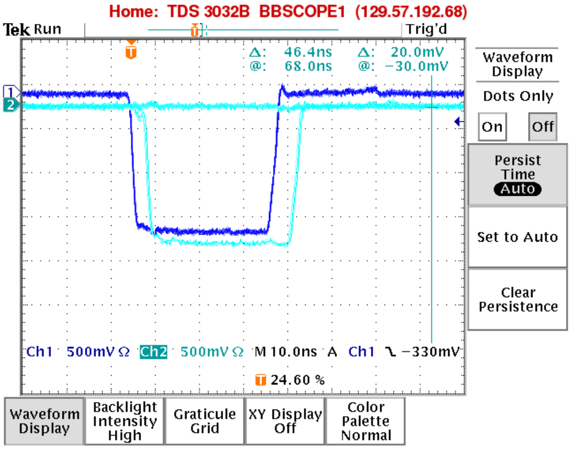


Figure 19: Plot shows the time difference between trigger T3 (blue) and T2(cyan) at the input to the scalers. The time difference between them is 4ns. That also means that time difference between the T1 and T2 on the input to the scalers is also approximately 4ns.

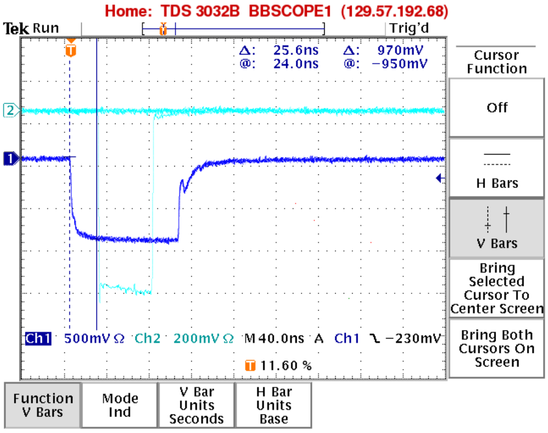


Figure 20: Plot shows time difference between final trigger T2(cyan) on the output from module PS-755 and trigger T3(blue) on the end of the cable from the HRS-L. Time difference between the two is 28ns. We already know that according to figure 8 T3-to scalers comes 23ns after T3 and that T3-to scalers comes 4ns before T2-to-scalers. By looking at figure 6 we also realize that T2-to scalers comes 3ns before T2. In the end this gives us $23 + 3 + 4 = 30ns$ difference according to schematics.

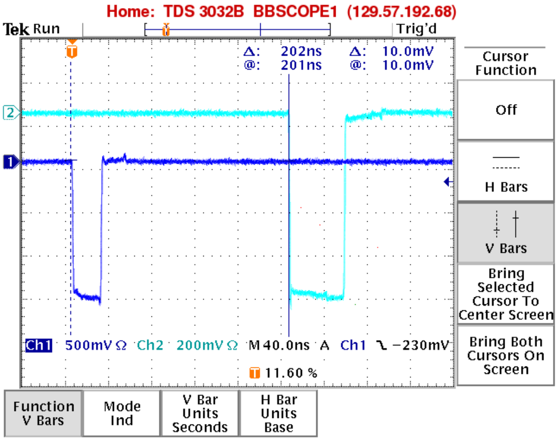


Figure 21: Plot shows the time required for the signal to come from the output of the module PS-754 module (figure 6) right after it comes from the module N408, to the trigger T2 output. Time difference was set to be 202 ns

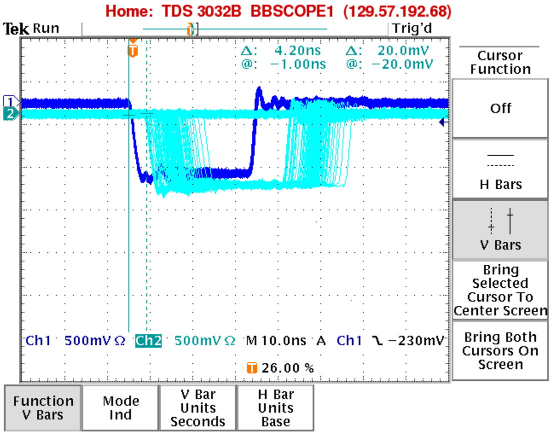


Figure 22: Minimal difference between the trigger T1(blue) and T2(cyan) on the input to the scalers is 4.2ns. The maximal difference between the two is 18ns, but this happens rarely.

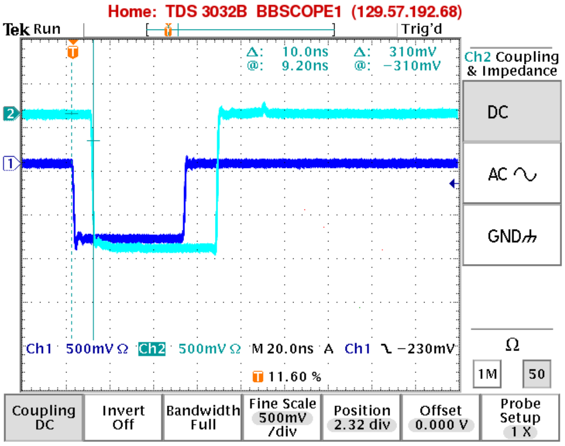


Figure 23: Time difference between signal (T1 or T2) on the output from module PS-755 and trigger T1 is approximately 10ns. According to figure 8 this time difference should be $8 + 1 = 9$ ns.

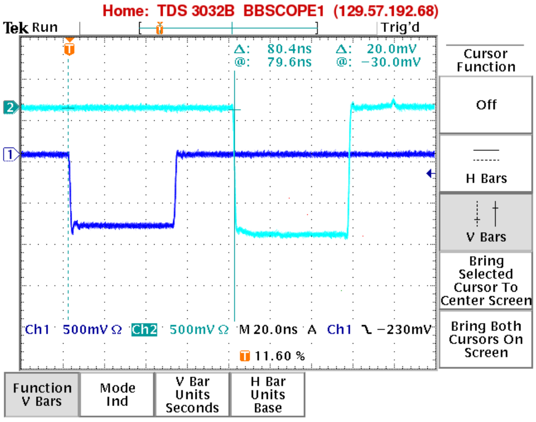


Figure 24: Plot shows the time difference between the T1(blue) on the output of the module PS-754 and $(T1orT2)_Delayed$ pulse on the output of the module PS-755 after the cable delay. The time difference is 80.4ns. According to figure 8 this time difference should be: $1 + 8 + 2 + 25 + 8 + 25 + 2 + 8 = 79ns$. This agrees quite well.

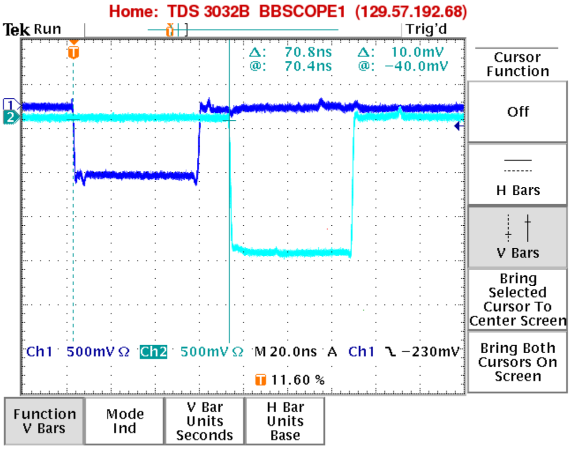


Figure 25: Plot shows the time difference between the (T1 or T2)(blue) on the output from the module PS-755 and $(T1orT2)_{D}elayed$(cyan) pulse on the output of the module PS-755 after the cable delay. The time difference is 70.8ns. According to diagram 8 this time difference should be: $2 + 25 + 8 + 25 + 2 + 8 = 70ns$. This agrees quite well.

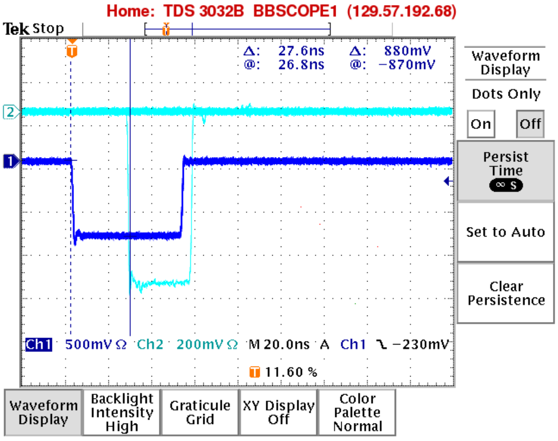


Figure 26: This scope plot shows time difference between trigger T1(blue) and coincidence trigger T5(cyan) which is approximately 27.6ns. Looking at diagram 8 we realize that this difference should be: $4ns + 10ns + 4ns + 8ns = 26ns$. This is good enough.

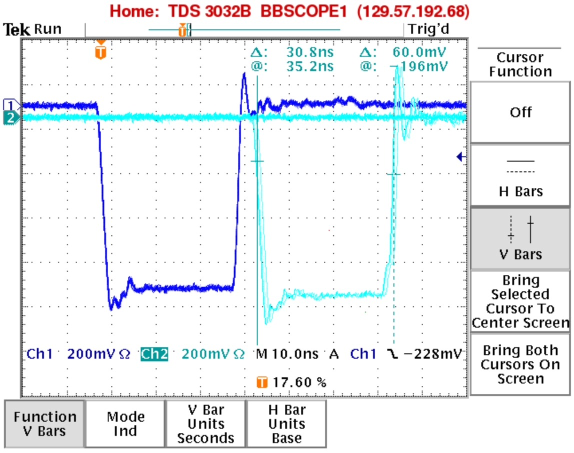


Figure 27: Plot shows time difference between trigger T3(blue) and T5(cyan) on the input to the scalers. Difference between the two is approximately 34ns. From the diagram 8 we know that trigger T3-to-scalers comes 23ns before T3, that T3 comes 26ns before T1, that T5 comes 26ns after T1 and that T5-to-scalers comes 7ns after T5. Putting all these findings together we get $26ns + 26ns + 7ns - 23ns = 36ns$ delay according to out diagrams.

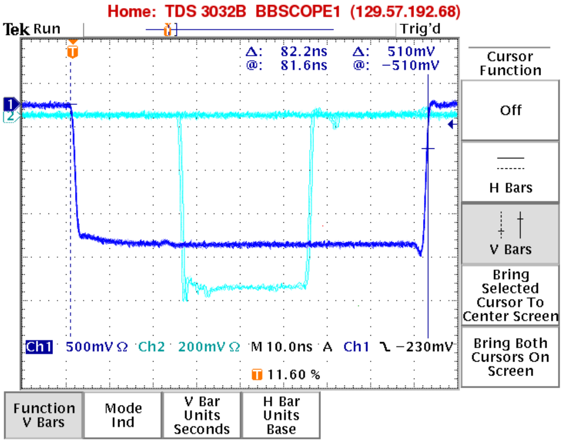


Figure 28: Plot shows coincidence trigger T5(cyan) relative to coincidence window (blue) made of T3. Coincidence window is 82ns wide and comes approximately 25ns before coincidence trigger happens. According to diagram 8 coincidence window should open $4+10+1+8 = 26ns$ after T3. We also know that T5 comes 28ns after T1 and that T1 comes 26ns after T3. This means that by looking at the diagrams the time difference between T3 and T5 should be 28ns.

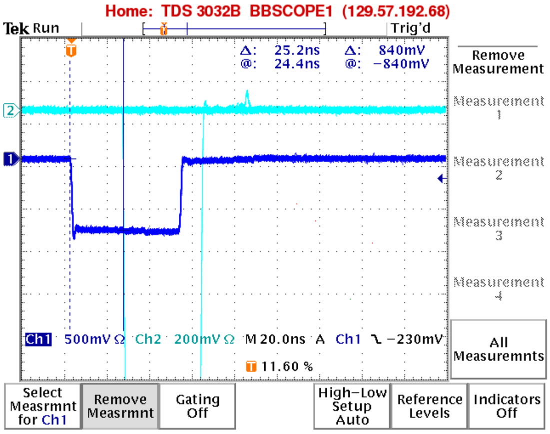


Figure 29: Plot shows time difference between trigger T2(blue) and coincidence trigger T6(cyan) which is approximately 25ns. According to diagram 8 this difference should be: $2ns+10ns+4ns+8ns = 24ns$.

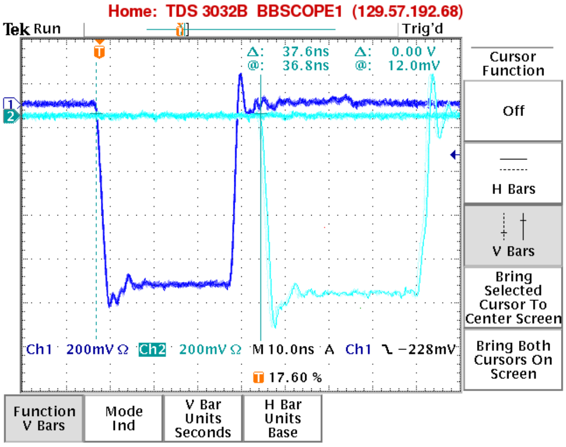


Figure 30: Time difference between trigger T3(blue) and coincidence trigger T6(cyan) on the input to the triggers is according to scope measurement 37.6ns. From the previous discussion we know that T3-to-scalers comes 23ns after T3, that T6 comes 25ns after T2, that T3 comes 28ns before T2 and that T6-to-scalers comes 7ns after T6. This means that time difference should be: $7ns - 23ns + 25ns + 28ns = 37ns$. This is very good.

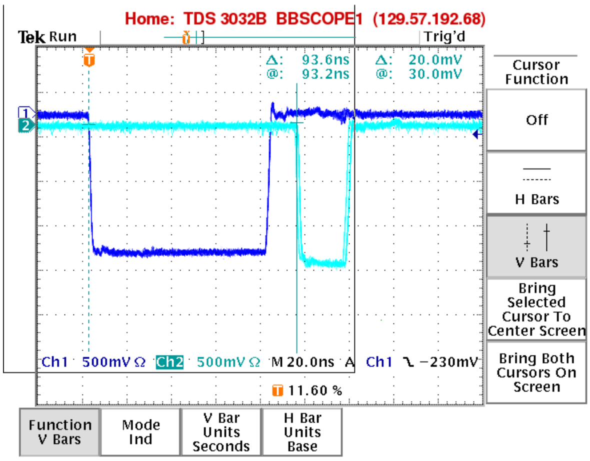


Figure 31: This scope plot shows the time difference between L1A and delayed L1A pulse which is used as supplementary BigBite re-timing pulse when there is no T1 or T2. The time difference is set to be 94ns.

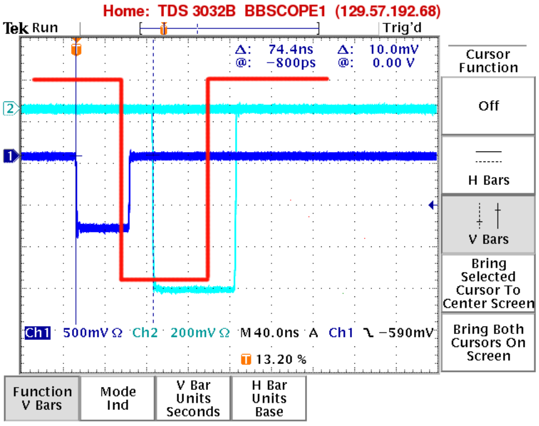


Figure 32: This plot shows the time difference between the trigger T1 (blue) and L1A pulse (cyan) for the case, when Trigger Supervisor accepts coincidence trigger T5. The time difference between the two is approximately 74ns. If the situation, where trigger supervisor would accept T1 or T3 (they come at the same time to the TS) as a valid pulse, than this time difference would be smaller. From the previous discussion we know that T1 comes approximately 38ns before T5. Consequently this means that L1A would also come 36ns earlier which than gives us: $74 - 36 = 38ns$. The L1A pulse for that situation is drawn on plot with red line.

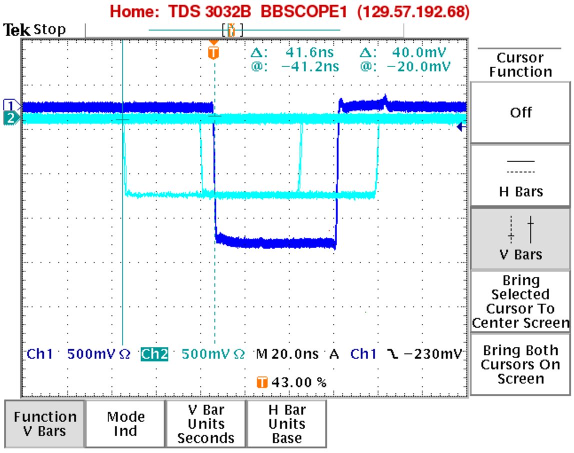


Figure 33: This scope plot shows the time difference between the L1A pulse(cyan) and $(T1orT2)_{Delayed}$ pulse (blue). We can see that we have to cases. In the case when TS accepts trigger T1 or T3, the time time difference is 42ns. In the case when TS accepts coincidence trigger is this difference 6ns. The difference between these two cases is exactly 36ns, which agrees with the time difference between T1 and T5 at the input to the scalers. This agrees with previous plots 24 and 32. The time difference between T1 and $(T1orT2)_{Delayed} = 80ns$, while the time difference between T1 and L1A is 74ns for the coincidence case. Subtracting these two numbers we get exactly $80ns - 74ns = 6ns$.

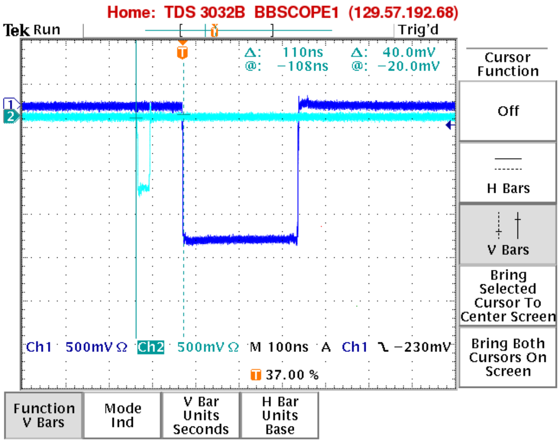


Figure 34: Plot shows the time difference between T1 and BigBite re-timing on the input to the scalers. The time difference is approximately 110ns. According to the electric scheme 9 the time difference should be: $1+8++25+8+25+2+8+1+8+1+5+1+3 = 103ns$. Since the error of our readout from the scope plot is at least 5ns this is a good match. From the plot we can also see, that position of the BigBite re-timing signal is not moving relative to the T1. This is the way that should be, since we designed our circuit so that BigBite re-timing pulse is always timed of T1.

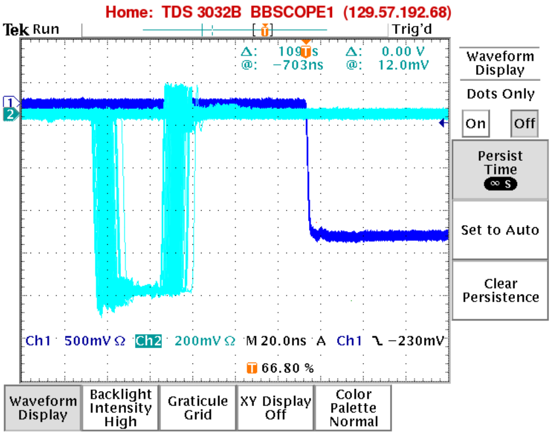


Figure 35: This scope plot shows the time difference between T2 and BigBite re-timing on the input to the scalers. The maximum time difference is approximately 100ns. Minimal time difference is 86ns. From previous plots we know that time difference between T1 and BigBite re-timing is 103ns. If we consider that according to plot 22 T2 comes between 4ns and 18ns after T1 we get almost identical numbers: $103 - 4ns = 99ns$ and $103 - 18ns = 85ns$.

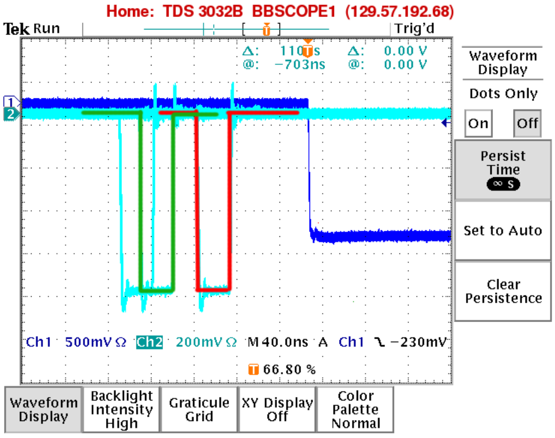


Figure 36: Plot shows the time difference between BigBite re-timing (blue) and trigger T3(cyan) on the input to the scalers. Since we do the re-timing always relative to T1, the time difference between T3 and BigBite re-timing is not constant, but is changing. We get three different peaks with time differences: 104ns, 156ns and 172ns. The first peak (red) corresponds to the situation, where we have both T1 and T3 triggers. Since we know, that they come to the scalers at the same time, the time difference between the T3-to-scalers and BigBite re-timing should be the same as the time difference between T1-to-scalers and BigBite re-timing, which is according to figure 34 103ns. The green peak on the other hand corresponds to the situation, where there is only T3. In this case we know, that L1A comes 37.4ns after T3. From schematics 9 we can conclude that BigBite re-timing comes $94 + 2 + 8 + 1 + 5 + 1 + 5 = 116ns$ after L1A. Together this gives us: $116 + 37 = 153ns$, which agrees with the plot.

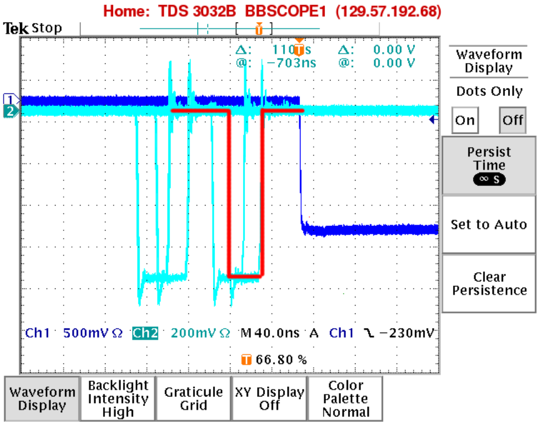


Figure 37: Plot shows the time difference between BigBite re-timing pulse(blue) and trigger T5(cyan) on the input to the scalers. we get multiple peaks which are result of multiple peaks in T3 (see figure 36). The valid peak is marked with red color and comes approximately 68ns before BigBite re-timing. This agrees with our previous findings. We know that time difference between T3-to-scalers and T5-to-scalers is 34ns and that time difference between T3-to-scalers and BigBite re-timing (for the coincidence case) is 104ns. This consequently gives us: $104ns - 34ns = 70ns$.

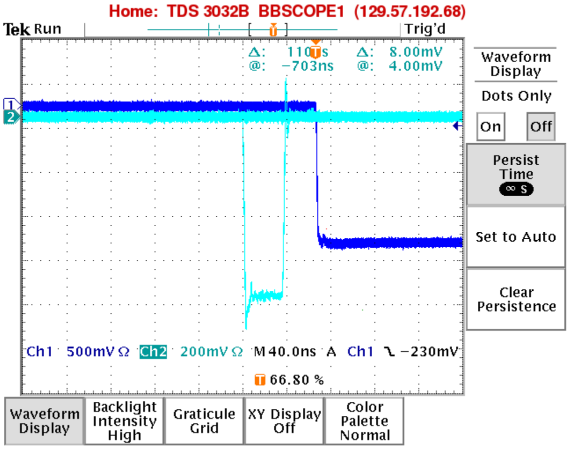


Figure 38: Plot shows the time difference between BigBite re-timing pulse(blue) and trigger T6(cyan) on the input to the scalers and measures approximately 68ns. We know from previous plots that T3-to-scalers comes 37ns before T6-to-scalers and that time difference between T3-to-scalers and BigBite re-timing (for the coincidence case) is 104ns. This consequently gives us: $104ns - 34ns = 70ns$ which agrees with this scope plot.

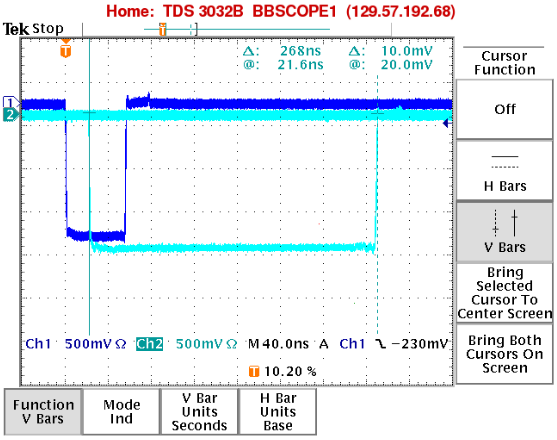


Figure 39: Time difference between BigBite re-timing pulse (cyan) and $(T1orT2)_{Delayed}$ (blue) is approximately 22ns.This agrees well with the scheme 9, according to which this difference should be: $1 + 8 + 1 + 5 + 1 + 5 = 21ns$.

5 Trigger TDC plots

Beside the tests that we made with the scope and simulated pulses we were also able to (as mentioned before) monitor the triggers through TDC spectra. Plot 41 shows the TDC spectra of triggers T1, T3 and T5 relative to the BigBite re-timing pulse for the deuteron run #2164. Looking at the plot we quickly realize, that it is far more complicated than we have anticipated. Let's try to explain where different peaks come from. Peak

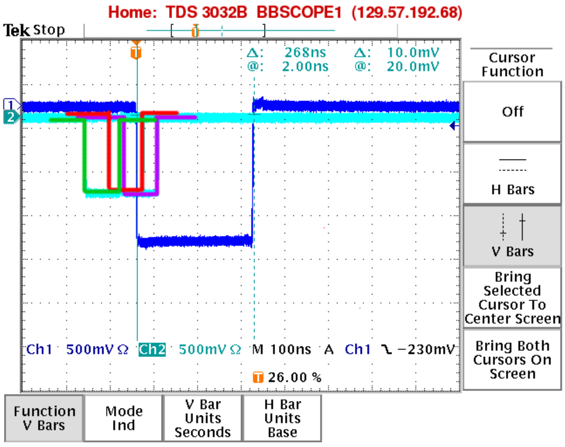


Figure 40: The width of the BigBite re-timing window(blue) i.e. width of the ADC-gate is 268ns. Plot also shows the time difference between BigBite re-timing pulse and L1A (cyan). As a result of different triggers and different situations we get three peaks with differences approximately 30ns (violet), 60ns (red) and 120ns (green). This can also be explained with help previous analysis. From plots 33 and 39 we know that L1A comes 6ns or 42 ns before $(T1orT2)_{Delayed}$ and that $(T1orT2)_{Delayed}$ comes 22ns before BigBite re-timing pulse. Summing these two numbers we get exactly what we need: $6 + 22 = 28ns$ and $42 + 22 = 64ns$. In the case when there is only T3 trigger, delayed L1A pulse opens the BigBite gate. Looking at the scheme 9 we get: $94 + 2 + 8 + 1 + 5 + 1 + 5 = 116ns$ which agrees well with the green line on scope plot.

$T3 - 1$ corresponds to the electron single events, where there was no detected proton/deuteron in BigBite. In this case, L1A pulse was timed off T3 and therefore this peak is sharp. Peaks $T3 - 1$ and $T3 - 1a$ correspond to coincidence peaks. We believe that the T3-1 peak represents coincidence protons, while the smaller T3-1a peak to its right represent elastic deuterons. We can see that the time difference between the T3-1 and T3-3 peaks is approximately 53ns. This difference agrees with the results from the scope test. If we subtract the time difference between T1 and the BigBite re-timing pulse shown on plot 3 from the time difference between T3 and the BigBite re-timing pulse for the T3-only case, we get exactly $156 - 103 = 53ns$. The T3-3 peak which is situated approximately 170ns before the BigBite re-timing pulse corresponds to the last peak on plot 41. We actually do not know where this peak comes from, but we can see that these events happen very rarely and can therefore be neglected.

Besides these three peaks in the T3 spectra we can also observe two sharp peaks T3-4 and T3-5 on the left side of the coincidence peaks. These two peaks also cause two additional peaks in the coincidence trigger T5 spectrum. Because the peaks are sharp, we can assume that in these two cases the BigBite re-timing pulse was timed off T3 instead of T1. When me make cuts around these two plots, we get the results shown in figure 42. From these plots we can see, that these two peak cause a plateau that we can observe on the right side of the T1 peak in graph 41. Since the distributions of the T1 are flat in these two cases these must be random events and contain no important physical content. From the detailed analysis of the scope plots we can realize that because of the different lengths of the pulses and delays it can in some random cases happen that the BigBite re-timing pulse is timed off T3 although there was a T1 present. For example: There is a single T3 event. While we are waiting for the delayed L1A pulse to form the BigBite re-timing pulse, a random T1 comes and it has just enough time to form the coincidence and come into the TDC, where it is read out. Since the events in these peaks (T3-4 and T3-5) are not important, we can make a cut on the trigger T3 and get rid of this background. Plot 43 shows all the triggers with the T3 cut: $T3 > 760$.

6 Conclusion

In this report I have described the triggers used during the E05-102 experiment for the combination of BigBite and HRS-L spectrometers. I have shown the electronics schematics for the triggers and BigBite re-timing and compared them with the scope plots and TDC histrograms. They seem to agree to the extent that we were able to check so far. Especially from the TDC plots we can see that in real spectra we get some additional peaks that we did not expect. However, we have found the origin of these peaks and proven that they are irrelevant to our experiment. Therefore we can conclude that the BigBite trigger worked properly.

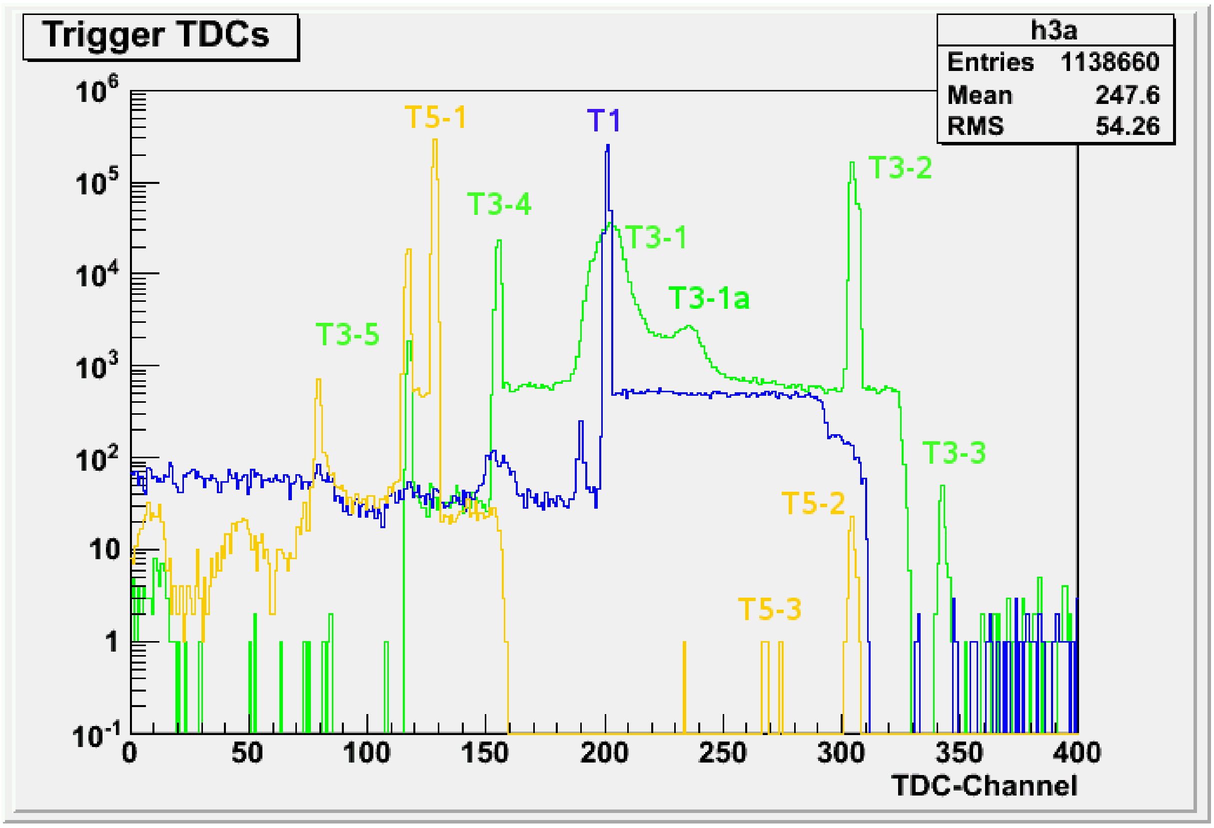


Figure 41: Plot shows the TDC spectra of raw triggers T1, T3 and T5 relative to the BigBite re-timing pulse.

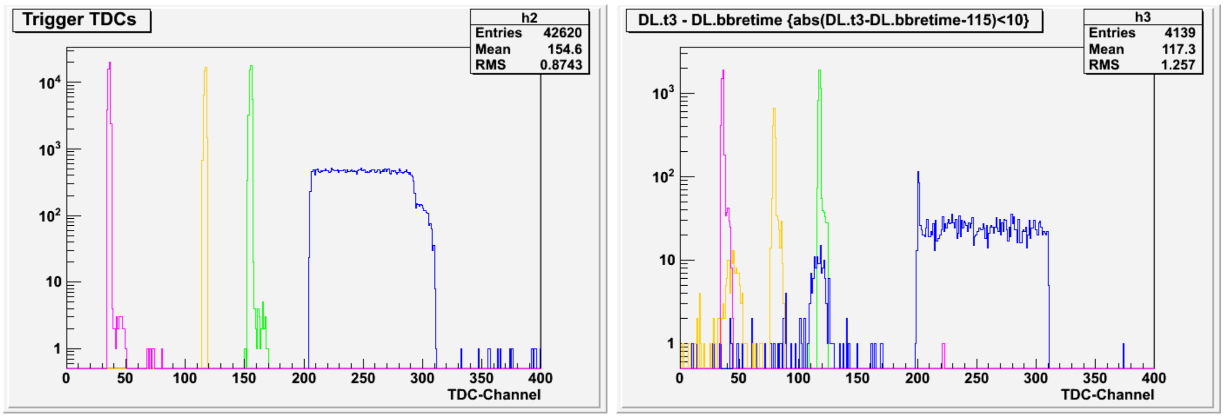


Figure 42: Left plot shows the T1, T3 and T5 triggers with cut $|DL.t3 - 760| < 10 \&\& DL.t1 > 805$. Right plot shows same triggers with cut $|DL.t3 - DL.bbretime - 115| < 10$. From the plots we can see, that in both cases is trigger T1 constant function. This means that physical events in these peaks but just random noise.

References

[1] D.J.J. Lange *et al.*, Nucl. Instr. and Meth. **A 406** (1998) 182

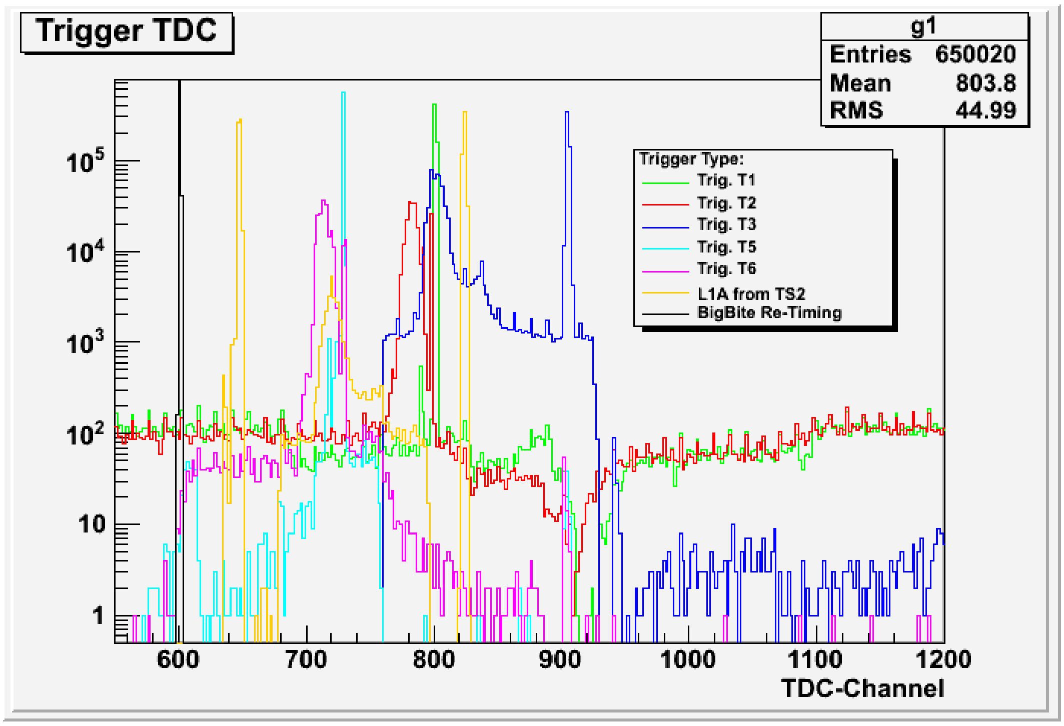


Figure 43: Plot shows the TDC spectra of raw triggers T1, T3, T5 and T6 and signals L1A and BigBite re-timing.